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|---|---|
| ENGLUND, T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

**DATE MAILED:** 03/14/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/188,241 | LUO, WENZHE | |
| | Examiner | Art Unit | |
| | Terry L Englund | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 1998* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

## DETAILED ACTION

### *Response to Request for RCE/Amendment*

The request for the RCE submitted on Dec 5, 2000 was approved, resulting in the amendment of Nov 15, 2000 being entered. That amendment was reviewed and considered with the following results:

Although page 1 of the amendment indicates copies of the substitute Abstract and the proposed drawing corrections have been submitted, those have not been located by the examiner. The TRANSMITTAL LETTER, which was submitted along with the amendment, clearly states "Transmitted herewith are an amendment... (7 Pages)." Since the amendment itself has only seven pages, were the abstract and drawings submitted on or with other documentation? If so, there is no indication (e.g. annotation on the filewrapper) the PTO has ever received them. Therefore, the examiner requests evidence that the substitute Abstract and drawing corrections had been submitted to, and received by, the PTO. Until copies are seen and reviewed by the examiner, the objections to the abstract and drawings will be maintained. Those objections are repeated later under the appropriate sections.

The amended changes to pages 2, 9 and 10 were entered after the examiner reviewed and corrected the line numbers for the changes to page 9. Since it is believed the changes have now been entered at the proper places, the objections to the disclosure have been withdrawn. [Although the amendment had identified the proper line numbers for pages 2 and 10, the cited line numbers for page 9 corresponded to neither the line numbers along the left margin of the page within the disclosure, nor the

actual line number (with respect to the first printed line on a page being considered as line 1). For example, the amendment indicated changes to lines 12, 18, 16 and 24 were to be made on page 9. However, the examiner had those changes made to respective lines 8, 14, 12 and 20 (according to the margin's numbering), which correspond to actual lines 7, 13, 11 and 19, respectively. [It is suggested that if any more amendments are to be made to the specification, the applicant should carefully review the page and line numbers to ensure they correspond to the actual copies submitted to the PTO.]

Amended claim 17 overcame its objection, which has now been withdrawn.

The amended claims, and/or comments, have overcome some of the rejections of claims 1-22 under 35 U.S.C. 112, second paragraph described in the previous Office Action. For example, the comments with respect to "substantially continuously" help clarify what the applicant means in claims 1, 18, 21 and 22. Although the use of "pull-down mirror path" and "pull-up amplifier" in claim 13 can be confusing, the comments on pages 4-5 of the amendment discloses the mirror path can be either a pull-down, or a pull-up amplifier (also disclosed on page 6, lines 5-8). Apparently, the applicant deems recited limitations of a "pull-down mirror path" comprising a "pull-up amplifier" as being acceptable. Therefore, the rejections under 35 U.S.C. 112 of claims 18, 21 and 22 (with respect to "substantially continuously"), and of claims 1-17, have been withdrawn. However, the amended claims have created some new rejections and some of the previous rejections of claims 18-22 have been maintained. All these remaining, and/or new, rejections are repeated later under the appropriate section.

All the prior art rejections, with respect to the reference of Harston, have been maintained. They are repeated later, with some modifications to account for the amended claims, under the appropriate section.

A reference by Ravon, found during a recent search, is used below for new prior art rejections under both 35 U.S.C. 102(e) and 35 U.S.C. 103(a). That reference is a patent which was issued Oct 24, 2000, almost two months after the Final Rejection was mailed. Therefore, it had not been available to the examiner. [It is also noted that the reference's filing date is Jun 3, 1998, which is prior to the Nov 9, 1998 filing date of the present application.]

Although the previous Office Action indicated allowable material. In claims 21 and 22, that indication has been withdrawn. The newly found reference of Ravon shows and discloses circuitry which reads on the claimed limitations. Therefore, prior art rejections of claims 21 and 22 are also described later under the appropriate section.

**Drawings**

The drawings remain objected to because Fig. 3 does not show the "numbers "0.5", "1.0" and "0.5" adjacent" the transistors as page 3, lines 21-24 describe. Figs. 3, 5, 6A, 6B and 8 show signal "IS" which is described as "/S" within the specification (e.g. page 3, line 20 and page 7, line 12). It is suggested the figures, or the specification be modified to ensure consistent labeling between the figures and specification. Fig. 2 does not show "Vo" described on page 4, line 6. Corrections are still required.

***Specification***

The abstract remains objected to because line 2 "having" should be --has-- to help improve word flow. The phrase "The disclosed embodiment" on line 4 is implied. Therefore, it is suggested the phrase "disclosed embodiment of the" be deleted. Corrections are still required. See MPEP § 608.01(b).

***Claim Rejections under 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 4, 10, 11, 15-17, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear in claim 3 how "a second load" (line 3) relates to "a first load" recited in claim 1 (line 5) because it now appears the current source switching circuit comprises two loads. Unless the applicant can clarify what two loads are being recited with respect to the applicant's figures, it is believed --said first load-- was meant in claim 3. After reconsidering the language of claim 10, the "being adapted for" phrase is deemed indefinite. It has been held that the recitation that an element is "adapted" to perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. ***In re Hutchison***, 69 USPQ 138; ***In re Ashley and Roberts***, 137 USPQ 361; and ***In re Rohrbacher and Kolbe***, 128 USPQ 117. Amended claim 15 now has a current sink (from claim 15) and a current source (from claim 2). However, it is no longer clear how the current sink and current source relate to the load.

For example, the applicant's Fig. 7 shows a current sink 720, and a current source 740, wherein Fig. 8 shows current source 740 is capacitor CL. Therefore, what does the applicant now consider as the load with respect to what is recited within claims 15-17? After reconsidering the language of claim 20, it is not known how "a load" relates to the current source/charged capacitor. Isn't the load the charged capacitor?

Claims 18-22 remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear in claim 18 how "reduce charge injection" of line 10 relates to "reducing charge injection" recited on line 1. If they relate to the same "charge injection", it is suggested the term --said-- be added prior to "charge" on line 10. The description "continuously receives said current flowing from said current source" in claims 21 (lines 8-9) and 22 (lines 9-10) is misleading. For example, the applicant's Fig. 5 shows current IA from current source 420 which would flow to load 440 only when transistor switch 430 is conducting. However, when transistor switch 430 is off, current IA would not flow to load 440.

Dependent claims carry over the rejection(s) from claim(s) upon which they depend.

***Claim Rejections under 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

In so far as being understood, claims 1-5, 8-10, 12, and 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ravon, a reference found during the recent search. For the following descriptions, Figs. 2-4 of Ravon will be considered and/or referred to, wherein one of ordinary skill in the art would be able to recognize the relationships between the figures. In Fig. 2, Ravon shows a current source switching circuit comprising a transistor switch M1; what can be deemed a pull-down mirror path M2,13,14 in parallel with transistor switch M1; and first load C'. Block 11 is a current source which is shown in detail in Fig. 3 (see column 4, lines 44-45). Fig. 4 shows load C', transistor M2, and details of comparator 14. Although transistor switch M1 is replaced by diode D1 in Fig. 4 (see column 6, lines 16-18), Ravon also discloses a transistor provides better efficiency on column 6, lines 16-18. Therefore, for the following description, diode D1 of Fig. 4 will be replaced with a transistor switch (e.g. M1 of Fig. 2) for improved efficiency, wherein block 13 of Fig. 2 will be used to control the on/off operations of both transistors M1 and M2. One of ordinary skill in the art would recognize that current source 11 (shown in Figs. 2 and 3) provides current I to terminal E of Fig. 4. Although the reference does not clearly disclose the "substantially continuously" reduction of "charge injection" as recited within the claims, one of ordinary skill in the art would know it relates to the current required to charge the load capacitor. When transistor M2 is off and transistor switch M1 is on, first load C' receives current I (from current source 11) through transistor switch M1 (e.g. see Fig. 2). Besides charging first load C', the current also charges capacitor C1 through resistor R1 (see

Fig. 4). [Note that the structure of first load C', capacitor C1, resistor R1, and amplifier 20 closely corresponds to the respective load 440, capacitor C1, resistor R1, and amplifier 400 structure of the applicant's Fig. 5.] When transistor switch M1 is turned off, and transistor M2 is turned on, capacitor C1 will help maintain the voltage across (i.e. between terminal S and ground) first load C', and less current will be required to completely charge first load C' back up once transistor switch M1 is turned back on. Therefore, transistor switch M1 and pull-down mirror path M2,13,14 substantially continuously reduce the charge injection into first load C', and claim 1 is anticipated. Fig. 2 clearly shows current source 11 connected between power source Vc and a first side E of transistor switch M1, and first load C' connected between ground and a second side S of transistor switch M1, thus anticipating claims 2 and 3. Since load C' is a charging capacitor, and transistor M1 is a MOS transistor, claims 4 and 5 are also anticipated. Transistor M2 of the pull-down mirror path M2,13,14 can be deemed a pull-down amplifier, anticipating claim 8. When transistor M2 is conducting, its output (i.e. drain) follows the current source 11 side of the transistor switch M1 by allowing the current to flow through transistor M2, thus claim 9 is anticipated. Transistors M1 and M2 receive their respective signals from control 13 (see Fig. 2) which allows transistor M2 to be turned off, and then transistor M1 to be turned on (see column 4, lines 28-30). Therefore, transistor M2 can be deemed a complementary pull-down mirror path transistor switch which operates opposite the transistor switch M1, anticipating claim 10. Since current source 11 comprises MOS transistor M3, claim 12 is anticipated. Transistor/switch M2 provides a pull-down mirror path parallel with current switch M1,

wherein switches M2 and M1 are substantially turned on and off alternatively, anticipating 18 and 19 because when transistor M1 is off, the capacitor C1 will basically maintain a voltage on load capacitor C', thus substantially continuously reducing the charge injection flowing to the load. Current source 11 comprises a charged capacitor C (see Fig. 3), thus anticipating claim 20. Transistor switch M1 connects current source 11 to load C', and it is substantially simultaneously turned off when switch M2 is turned on. When switch M2 is on, the current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C', the charge injection will be reduced when transistor switch M1 is opened, and claim 21 is anticipated. The upper output of block 13 is coupled to the gate of transistor switch M1 and is deemed the means for opening transistor switch M1, and the lower output of block 13 is coupled to the gate of switch M2 and is deemed the means for closing switch M2, wherein current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C', the charge injection will be reduced when transistor switch M1 is opened, and claim 22 is anticipated.

**Claim Rejections under 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to respective claims 1 and 10 above, and further in view of the applicant's Prior Art Fig. 3. As described previously, the basic current source switching circuit is shown and disclosed by the reference of Ravon. However, the reference does not show or disclose the use of the serial combinations of transistors as recited within claims 6, 7 and 11. Ravon shows only a single transistor for transistor switch M1 and for complementary pull-down mirror path transistor switch M2. It would have been obvious to one of ordinary skill in the art to replace each of transistors M1 and M2 of Ravon's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection. Since Ravon's circuit can be considered a current type switch circuit for charging first load C', the compensated switch of the applicant's Fig. 3 would help reduce charge injection even more within the circuit if that was desired.

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to claim 1 above. As described previously, Figs. 2 and 4 of Ravon

show a circuit with a transistor switch M1, pull-down mirror path M2,13,14, current source 11, and first load C'. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuitry of Ravon by reversing the polarities (i.e. Vc and ground would be reversed) and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage (e.g. closer to power source Vc). The reversal would replace all the MOS transistors (i.e. M1-M6) with their complementary transistors (i.e. an NMOS transistor would be replaced with a PMOS transistor). In this case, transistor M2 would be coupled between power source Vc and the common connection of current source 11/transistor switch M1, and first load C' would be coupled between power source Vc and terminal S. Therefore, transistor M2 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 11 would be coupled between ground and one side E of transistor switch M1, rendering obvious claim 14. Since current source 11 would be sinking current to ground, it could be deemed a current sink coupled between ground and one side E of transistor switch M1, rendering claims 15 and 16 obvious. The circuit would comprise charging capacitor C', coupled between power source Vc and one side S of transistor/current switch M1, rendering claim 17 obvious.

In so far as being understood, claims 1-5, 8-10, 12, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harston, the reference cited in the previous Office Action. In Fig. 3 Harston shows a current source switching circuit comprising transistor switch MP2; a pull-down mirror path MP3 in parallel with said transistor switch MP2; and first load 10pf. Although the reference does not clearly disclose a reduction in charge injection, it would be obvious to one of ordinary skill in the art that resistor 37.5Ω would reduce the charge injection flowing to first load 10pf

because it will start discharging first load 10pf when transistor switch MP2 is turned off. Therefore, as long as transistor switch MP2 is off, and there is a charge on first load 10pf, the charge injection flowing to the first load will be substantially continuously reduced, thus rendering claim 1 obvious. [MP3 is considered a pull-down mirror path since it mirrors the operation of the transistor switch MP2 and allows the current from transistor MP1 to flow down to ground. See column 2, lines 64-68.] Fig. 3 also shows a current source MP1 (a MOS transistor) coupled between power source CURRENT CELL and the first side of transistor switch MP2; and load 10pf is a charging capacitor 10pf coupled between ground and a second side of transistor switch MP2, thus rendering obvious claims 2-5. Since a transistor can be deemed an amplifier, pull-down mirror path MP3 can be deemed a pull-down amplifier, rendering claim 8 obvious. When transistor MP3 is conducting, its output (i.e. drain) follows the current source MP1 side of the transistor switch MP2 by allowing the current to flow through transistor MP3, thus rendering obvious claim 9. Transistors MP2 and MP3 receive their respective signals DATAB and DATA. Therefore, transistor MP3 can be deemed a complementary pull-down mirror path transistor switch which operates the opposite of transistor switch MP2, rendering claim 10 obvious. It is complementary since it receives a control signal which is a complement of the signal received by transistor switch MP2. Since current source MP1 is a MOS transistor, claim 12 is rendered obvious. Transistor/switch MP3 provides a pull-down mirror path parallel with current switch MP2, wherein switches MP3 and MP2 are alternatively on and off, rendering obvious claims 18 and 19 because when transistor MP2 is off, the resistor 37.5 will discharge load 10pf, thus substantially continuously reducing the charge injection flowing to the load.

Claims 6, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to claims 1 and 10 above, and further in view of the

compensated transistor switch of the applicant's Prior Art Fig. 3. Harston shows only a single transistor for each of transistor switch MP2 and complementary pull-down mirror path transistor switch MP3. It would have been obvious to one of ordinary skill in the art to replace each of the single transistors MP2 and MP3 of Harston's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection of switches in analog circuits. Since Harston's circuit in Fig. 3 can be considered a current switch circuit related to an analog circuit, the compensated switch of Fig. 3 would help reduce charge injection within the circuit if that was desired.

Claims 13-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to rrespective claims 1 and 18 above. As described previously, Fig. 3 of Harston shows a circuit with a transistor switch MP2 (30), pull-down mirror path MP3 (32), current source MP1 (20), and load capacitor 10pf. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuit of Fig. 3 by reversing the polarities and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage. The reversal would replace all the PMOS transistors (i.e. MP1, MP2 and MP3) with NMOS transistors. In this case transistor 32 would be coupled between power source CURRENT CELL and the

common connection of current source 20 and transistor switch 30. Therefore, transistor 32 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 20 would be coupled between ground and one side of transistor switch 30, rendering obvious claim 14. Since current source 20 would be sinking current to ground, it could be deemed a current sink coupled between ground and one side of transistor switch 30, rendering claims 15 and 16 obvious. The circuit would comprise charging capacitor 10pF, coupled between power source CURRENT CELL and one side of transistor/ current switch 30, rendering claim 17 obvious. Deeming capacitor 10pF a current source, claim 20 is rendered obvious. It would charge up to CURRENT CELL when transistor 32 conducts, and discharge (or supply current) when transistor 30 conducts.

No claim is allowable as presently written.

***Response to Arguments***

The applicant's arguments filed Nov 15, 2000 have been fully considered but they are not persuasive. The applicant argues: 1) claim 18 clearly set out the "charge injection" limitations within claim 18; 2) current is continuously received by the load after opening a transistor; 3) Harston fails to disclose a transistor switch and a pull-down mirror path; 4) Harston's current flows to ground and there is no mirror path; and 5) Harston does not teach a reduction of charge injection as claimed.

1) The applicant argues that the preamble of claim 1 recites "reducing charge injection" and line 10 recites "reduce charge injection." Although that may be true, the two uses of "charge injection" are not clearly distinguished from, or with, each other within the claim. For example, the charge rejection related to the current source may not be the same as the charge rejection flowing to the load, since the load could

possibly be affected by charge injection from other circuitry. Therefore, it is suggested the charge injection through a current switch, and the charge injection flow to the load be more clearly described.

2) In response to the applicant's argument that the load continues to receive current after a transistor switch is open, the examiner requests better clarification on how the load can continuously receive current from the current source even when the only current path between the current source and load is opened as claims 21 and 22 indicate. For example, transistor switch 430 of the applicant's Fig. 5 is the only way current IA from current source 420 can flow to load 440. Therefore, once switch 430 is opened, how can current IA be continuously received by load 440?

3) . The applicant argues that the reference of Harston fails to disclose a transistor switch and a pull-down mirror path for reducing charge injection to a load. However, the examiner has clearly identified transistor MP3 as the pull-down mirror path which is parallel to transistor switch MP2. As long as transistor MP2 is off, and transistor MP3 is on, the charge injection (e.g. current) flowing to load 10pf is continuously reduced. In fact, the current is reduced to zero.

4) In response to the applicant's argument that the reference of Harston fails to show certain features of the applicant's invention, it is noted that the features upon which the applicant relies (e.g., mirror path current flow to the load; and continuous reduction of charge injection) are not clearly recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057

(Fed. Cir. 1993). In this case, the operation of transistors MP2 and MP3 of Harston can be considered mirrored because one transistor is off while the other transistor is on. Therefore, transistor MP3 can be considered a mirror path with respect to transistor MP2. As presently recited, the claims do not clearly recite a current must continuously flow to the load, and they do not indicate when the "substantially continuously" reduction of charge injection actually occurs. Therefore, as long as Harston's transistor MP2 is off, and transistor MP3 is on, the charge injection (e.g. current) flowing to load 10pf is continuously reduced.

5) The applicant argues that Harston does not teach a reduction of charge injection as claimed. However, one of ordinary skill in the art knows charge injection relates to charging current(s). Even though Harston does not specifically disclose the reduction of charge injection, one of ordinary skill in the art can consider less current, or no current as one type of charge injection reduction. In either case, the charge injection will be reduced from the normal charge injection current amount used to charge the load capacitor back up completely. Therefore, when transistor MP2 of Harston is open, how can there be charge injection to the load when there is no current flowing to the load?

The applicant's arguments with respect to claims 1-20 are considered moot in view of the new ground(s) of rejection with respect to the newly found reference of Ravon. As described within the formal rejections cited above, Ravon's capacitor C1 will help maintain the voltage dropped across load capacitor C'. When transistor M1 (in place of diode D1) of Fig. 4 is closed, both load capacitor C' and capacitor C1 will charge to approximately the same amount. When transistor M1 is opened, capacitor C1

helps maintain the voltage at terminal S, and when transistor M1 closes again, it will take less time and current to full charge up load capacitor C'. Therefore, the reference of Ravon shows/discloses circuitry, and a method, for "substantially continuously" supplying current to reduce charge injection flowing to the load C'.

For the reasons described above, the rejections are deemed proper with respect to the interpretation of the claim language and prior art references.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for this Art Unit is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

28 February 2001

/TIMOTHY P. CALLAHAN/
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800